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BERTScope-Based Signal Integrity Compliance Testing

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Abstract

Signal integrity compliance testing varies from application to application, but recurring themes are emerging to help multi-gigabit systems designers assure interoperability. Most of the tests needed to qualify a part or system can be performed with bit error rate testers and oscilloscopes; however a new generation of instrument, a BERTScope, takes advantage of naturally deep measuring capability, an integrated pattern generator (with calibrated stress), tightly-coupled eye diagramming, and bit error rate measuring functions to provide complete compliance testing.

This paper describes the measurements necessary for compliance testing as well as the features and benefits of the BERTScope for this application. Measurements of transmitter jitter, channel performance and receiver tolerance are described.

Author Biography

Tom Waschura is Chief Technical Officer and Founder of SyntheSys Research, Inc. He has designed bit error rate testers since 1984 and has a number of key inventions revolutionizing the use of bit error rate testers for expanded signal integrity analysis measurements. As CTO of SyntheSys Research, Tom motivates identifying and developing the technology behind the company's successful instruments and works to transfer this technology into products. Tom also works with the testing efforts for various standards including those from IEEE, ANSI, JEDEC, and OIF. Mr. Waschura has degrees from Hiram College, M.I.T., and Stanford University.

Introduction

Engineers that work with signal integrity compliance testing are no strangers to bit error rate testers and sampling oscilloscopes. Combined, these instruments stimulate and analyze the waveform properties, eye diagrams, jitter, and bit error rates typically used to specify a device or system. As data rates go higher and higher and problems get more and more difficult, the tests and test setups required to stimulate and measure signal integrity performance get more complex.

Integrating these two devices is a natural evolution encouraged by the inherently high effective sampling rate found in the bit-for-bit processing of a bit error rate tester. Exotic semiconductors and design techniques used to create ultra-high performance circuits necessary for instrument-grade data analyzers are also natural for creating analog samplers used to distinguish far more than simple I/O logic decisions. Legacy problems with older bit error rate testers that limited their effectiveness for more sophisticated analysis, including poor return loss, bandwidth, time base monotonicity/resolution, and user interface, have been overcome.

This integration and high performance, combined with the need for ever-migrating signal integrity analysis, thrusts the BERTScope to the forefront of flexible instruments that can make today's measurements and adapt to tomorrow's upcoming standards.

What is a Compliance Test for Signal Integrity?

Compliance tests vary from interface standard to interface standard and may involve both electrical and optical elements. These tests typically are comprised of transmitter, receiver, and channel measurements, and involve measurements of the device under test, as well as measurements of the test signals, to establish calibration. Examples of standards that call out various types of signal integrity compliance tests include 10 Gb Ethernet, Fiber Channel, Serial-ATA, Infiniband, PCI-Express, SONET, and XFI.

Transmitter measurements for compliance testing typically involve studying the transmitted waveform shape and intrinsic jitter. Receiver measurements include input jitter tolerance and sensitivity tests, often combined into long-term "four-corners" bit error rate tests. Channel measurements include knowing the eye opening impacts at a receiver caused by channel insertion loss characteristics. Failures in any area of these measurements prompt the additional need for diagnostic information to help sort out and solve problems. All these measurements are part of compliance testing for signal integrity.

Compliance measurements are designed to assure virtually error-free data transfers between devices or systems. This is truly a difficult task, as devices and systems are typically used for years, while test time for electronics is typically minutes (or seconds). To do this, large measurement populations are needed, and carefully thought-through extrapolation techniques that model the physics of the situation need to be accurately employed. Extrapolation techniques need further study to understand the error terms present. Still, it is clear that the deepest measurements possible need to be made to yield the least amount of error.

BERTScope Introduction

Many test instruments measure or infer data transmission quality. These include deep-memory real-time oscilloscopes, high-bandwidth sampling oscilloscopes, time interval analyzers, and bit error rate testers. Of these, only the bit error rate tester actually directly measures the bit error rate. For this reason and because of the need for a pattern generator in many test situations, bit error rate testers are typically present in some fashion for compliance test. With this a given, the next question would be to identify if any one bit error rate test architecture offers specific advantages over any other, and to understand if other tests typically not performed on a bit error rate tester could be.

The BERTScope product is a full-featured bit error rate tester that is easy to use and has all the normal features found in a high-performance BERT, including a flexible pattern generator, clock synthesizer, and error detector. It has a static-protected precision differential input built from Indium Phosphide and an accurate time base that measures intrinsic jitter to levels that require optional “enhanced” time bases on other instruments. It has internal time step resolutions as small as 20 femtoseconds, with time base monotonicity assured by built-in self-calibration circuits that recalibrate in seconds whenever data rate or temperature changes demand it.

The input of the BERTScope has been intelligently designed to allow direct voltage sampling of the signal along with threshold level detection needed for bit error rate measurements. The direct voltage sampling is achieved by creating a window comparator that counts the number of occasions where the applied signal is between two programmed thresholds at the instant defined by the time base. By sweeping the threshold voltages and time base throughout the eye extents, a two-dimensional probability density function is directly measured. This function, an eye diagram, collects samples into the population at a rate that depends greatly on the data rate and the number of pixels in the eye diagram. For instance, a 400x250-pixel image of an eye diagram for a 10 Gbit/sec stream would permit 100,000 samples at each pixel every second. This is thousands of times more efficient than sampling oscilloscopes, providing a deeper, more-complete eye diagram.

Similarly, by carefully choreographing the movement of the decision threshold and time base, mask testing can be performed. Mask testing checks the extents of the eye diagram against a user-defined mask template. These templates define regions that the signal should avoid. Anytime a signal is found within the masked region, a mask violation is declared. Mask testing with a bit error rate test engine is many thousands of times faster than mask testing using a sampling oscilloscope, which allows previously long mask tests to be completed in seconds.

The BERTScope also has an optional integrated stress generator feature built into its pattern generator. By using this function, the output data from the BERTScope can have calibrated stress added to it. For example, this includes being able to add timing jitters such as white noise, sinusoidal jitter and bounded-uncorrelated jitter (band-limited PRBS jitter). The output signal can also be interfered with by summing a programmable sine wave in either common or differential mode. These various stresses and the associated ranges and resolutions provided by the BERTScope allow for easy creation of stressed eyes for receiver tolerance testing.

Additionally, the BERTScope has the unique ability to make measurements in live traffic as well as with the normal repeating patterns. This innovation, another found only on the BERTScope, allows deep measurement analysis to be performed on systems running live traffic just as easy as making component measurements during production tests.

Intrinsic Jitter Measurement (Jitter Generation)

Intrinsic jitter is the natural jitter present in a transmitter's data stream. Depending on the sophistication of the jitter measuring technique called out in the standard, this can be an easy or difficult measurement. Early intrinsic jitter measurements made simple oscilloscope eye diagram measurements of jitter. This was found to be dominated by jitter introduced by the oscilloscope system, and today's standards often call out much more complicated time-domain or frequency-limited measurement methods for jitter, including separating random and deterministic jitter components.

To measure intrinsic jitter, standards typically define a specific test pattern (or patterns) to use when the jitter is measured. This signal is output from the device under test, and variations in the times of the edges found in the data stream, compared to their ideal times, are identified and measured.

The source of the 'ideal' edge locations for this comparison is the first issue that must be chosen. Ideal edge locations can be determined by recreating a clocking signal from the data signal (e.g., a phase lock loop clock recovery system). In these devices, a phase variation low-pass filter is used to find the average ideal edge locations, down to some low variation frequency where the filter in the phase locked loop is no longer useful.

Jitter analysis can often also be performed by using a known clean transmitter clock as the timing reference for the receiver. Avoiding the use of clock recovery, this approach is limited to applications where the timing of the transmitted signal is not expected to change through the DUT (e.g., Fully Buffered DIMM, Serial ATA, etc.)

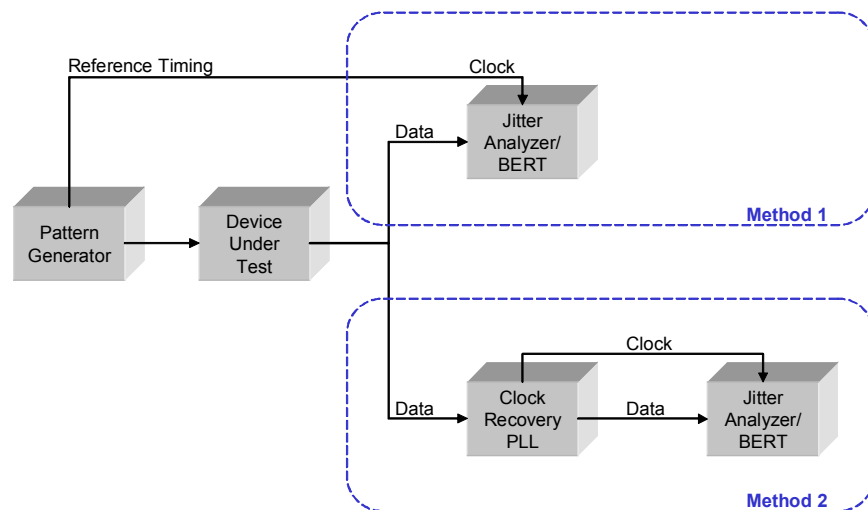


Figure 1: Two methods of measuring jitter. Use of clock recovery introduces jitter filtering by the phase lock loop (PLL).

Band-limited, PLL-based jitter measurements (e.g., SONET) measure the jitter that matters to the receiver; the frequency roll-off point of the PLL is chosen to match the tracking bandwidth of the PLL in SONET receivers. Jitter component separation is typically used in systems where significant deterministic jitter is present (e.g., from bandwidth limits in the transmission paths, such as FR4 backplanes or low-performance cables). This is useful because large amounts of deterministic jitter can be tolerated; however, large amounts of random jitter cannot.

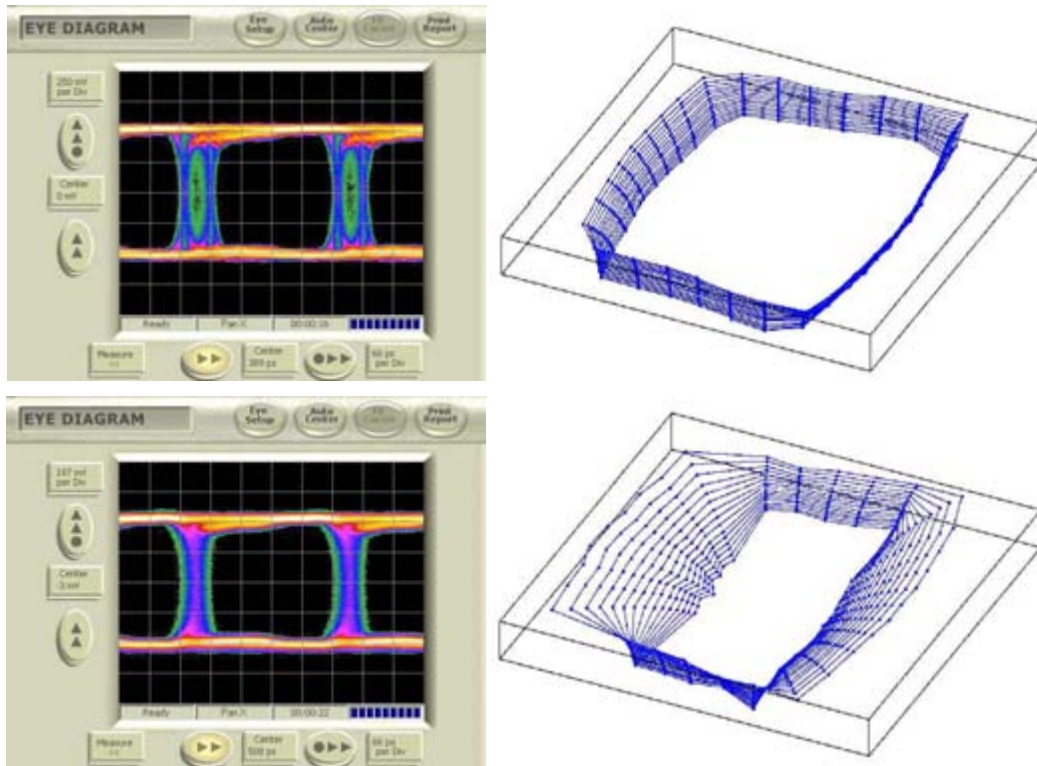


Figure 2: Measurements of two different systems – the upper one is dominated by deterministic jitter mechanisms, with impairments that occur frequently and are all visible in the eye diagram. The lower system is dominated by random jitter, and the eye only displays the frequently occurring events. A deeper view based on BER Contour shows that significant eye closure is present from low probability events that would cause the system to fail.

A BERTScope can use a hardware clock recovery module to create a recovered clocking signal. This clocking signal is then used by the input circuitry as the timing reference from which all jitter analysis is performed. This efficient jitter analysis can yield deep jitter measurements quickly because the hardware clock operates at the full, real-time bit rate. Jitter measurements include RMS and peak-to-peak jitter (provided either as an actual measurement, or extrapolated to a user-defined bit error rate).

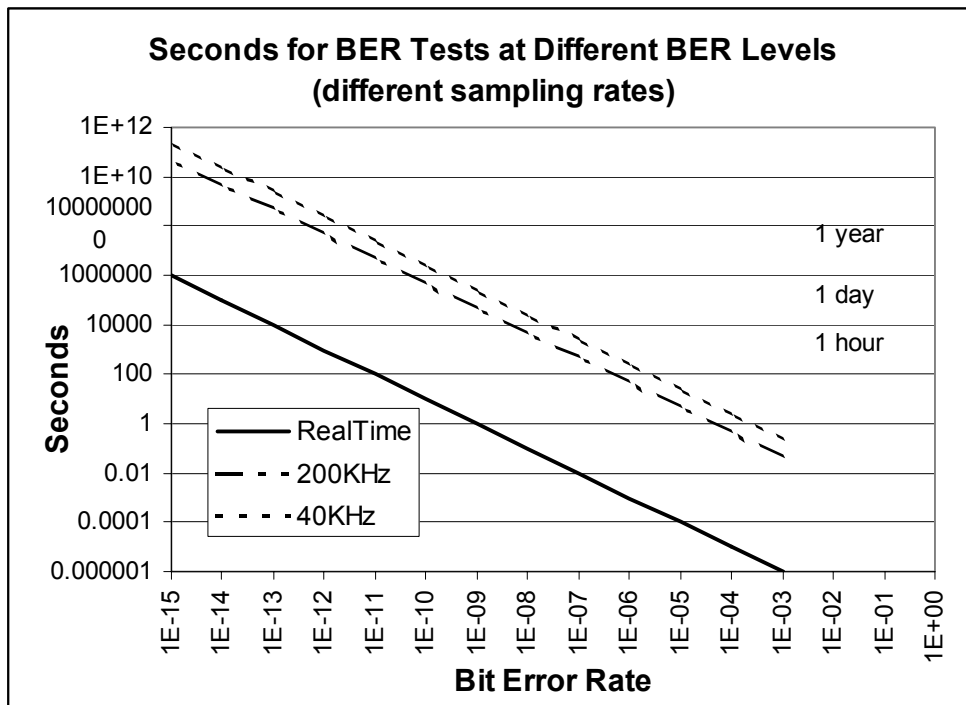
Measurements also include the separation of random and deterministic jitter as defined by the popular Dual-Dirac method¹. When making these measurements with long test patterns, it is now well understood that deep measurements must be taken or else wrong results will be obtained. The BERTScope, running at the full data rate of the channel, makes the deepest measurements possible, and its built-in time calibrations enable a time base accuracy that assures good jitter separation and extrapolation.

Bit Error Rate Measurement

Bit error rate is the rate at which errors are found between the transmitted/received data and the expected data. To perform this measurement, a known test pattern is used, and mismatches between the received data and the test pattern are counted/accumulated. For modern standards, this test requires monitoring every bit that goes through the device under test.

A bit error rate tester like the BERTScope does this by comparing every received bit against the known test pattern at the full data rate of the system. As many standards require the absence of bit errors down to 1×10^{-12} level (or better), typical test protocols require the passage of at least a few times 1×10^{12} bits to make sure. For example, in a 10 Gbit/sec system, a few multiples of 100 seconds in test time are needed to have a confident measurement, as shown in the following graph

Instruments based on sampling architectures, such as time interval analyzers and oscilloscopes (both deep-memory real-time oscilloscopes and high-bandwidth sampling oscilloscopes) have low effective sampling rates (40 kHz to 200 kHz), which make a full bit error rate test impractical due to their low efficiency.



Jitter Tolerance Measurement (Stressed Eye)

Jitter tolerance is a measurement of a receiver's ability to operate in the presence of jitter. This measurement requires a flexible pattern generator that can add prescribed amounts of jitter of various types on top of the test data pattern. This stressful data is then presented to the receiver and the received data is checked for bit errors using a bit error rate tester (or an internal bit error checker).

Stressed eye tests have evolved significantly in the past 10 years. Original systems added sinusoidal jitter to the test pattern; new specifications add jitter with various amounts of sinusoidal, random and uncorrelated-deterministic components on top of signals that often also have voltage interferences summed with them.

The method for making this measurement requires that you find the amount of stress that can be added before the bit error rate of the system exceeds the specification limit. Jitter tolerance tests often evaluate many frequencies of inserted jitter, and typically are specified as a template of the amount of tolerable jitter versus frequency.

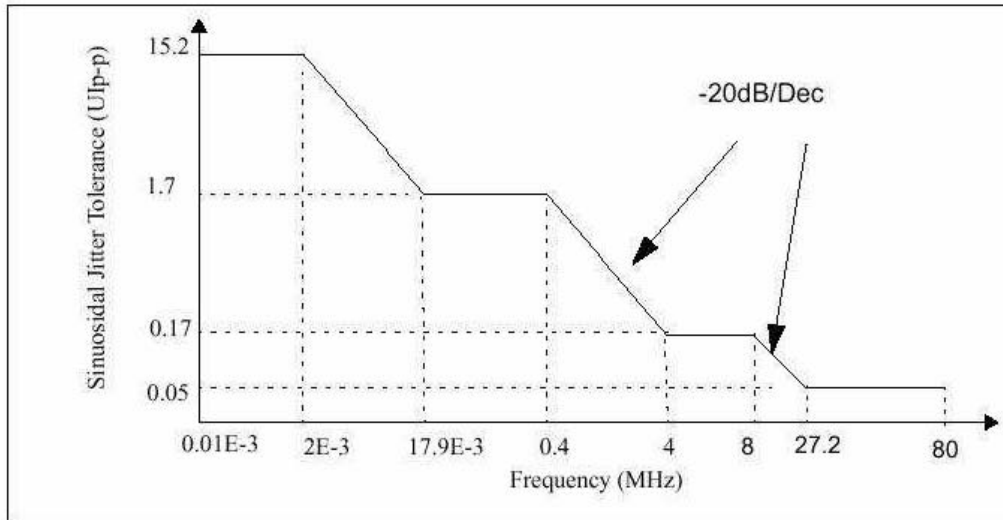


Figure 4: Example Receiver Jitter Tolerance Template²

The BERTScope has an optional stress insertion function that allows adding both internal and external jitter sources, as well as adding sinusoidal voltage interference. The internal jitter sources include sinusoidal jitter (up to 80 MHz), random jitter (white noise) with bandwidth from 10 MHz to 1 GHz), and bounded-uncorrelated jitter from a separate non-coherent PRBS generator which is band-limited to 25, 50, 100, or 200 MHz, to produce a jitter probability distribution that is bounded.

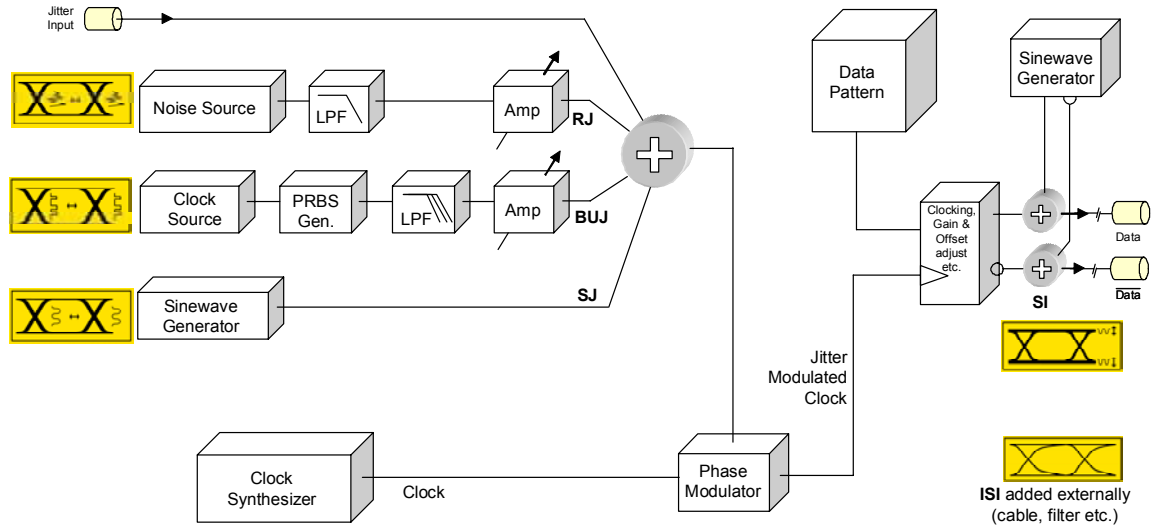


Figure 5: Block diagram of stress insertion capability

Because receiver tolerance tests require sweeping stress amplitudes and measuring many bit error rates, these tests are also best automated for efficient results. Additionally, the search algorithms used for these tests can be optimized as long as proper consideration is taken of the hysteresis present in most receiver clock and data recovery circuits.

The most difficult part of the stressed eye tolerance test is the calibration of the transmitter such that the proper amounts of stress of the various types are added. Incorrect amounts of stress may cause reduced production margins or, worse, may cause bad components to be passed. The BERTScope system offers calibrated stress, relieving the engineer of this difficulty.

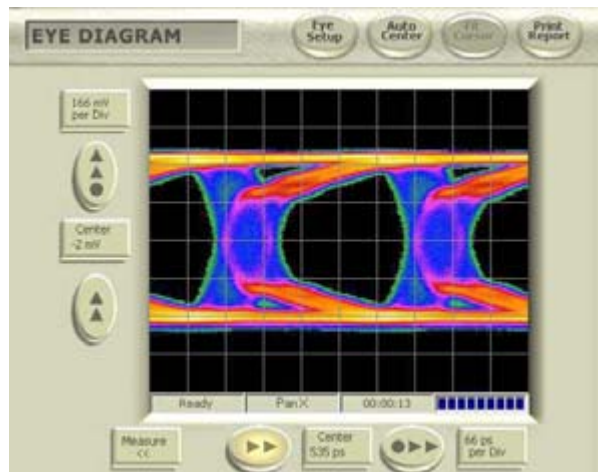


Figure 6: Example stressed eye used for receiver jitter tolerance testing

Channel Eye Opening Measurement

During development, the eye openings that remain after a long, lossy channel (e.g., an FR4 backplane or a low-cost cable assembly) are often simulated with S-parameter-based methods such as the ones developed by the open source StatEye team³. StatEye software convolves the responses of a transmitter's characteristics with the measured S-parameters of a channel to predict the bit error rate contour of the eye opening at the receiver. Verification of the real-life channel behavior for low-probability events must then be analyzed with deep measurements.

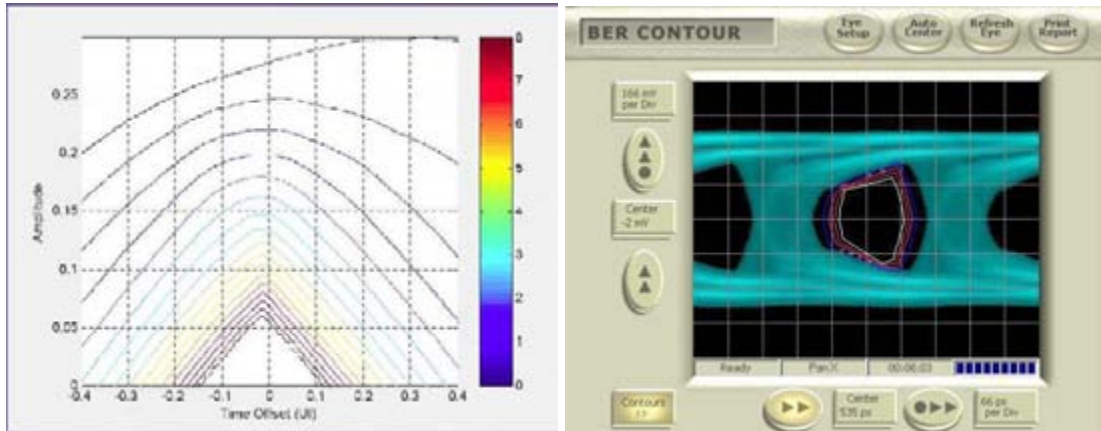


Figure 7: A BER Contour prediction from using StatEye (left) and an example measured BER Contour

The BERTScope allows choices between deep eye diagrams, BER contours, horizontal timing jitter peaks (BER bathtub curve), or vertical voltage Q-factor analysis. Each analysis is specialized to uncover different characteristics about the signal.

For channel measurements, it is often desired to understand the data-dependent jitter impacts that come from the frequency-domain insertion loss of the channel (summed with any impacts of return-loss mismatch and noisy neighbor transmissions). This can have an impact in the horizontal uncertainty analyzed with jitter analysis, and can also have impact on the vertical eye closure that is well-analyzed by the Q-factor analysis.

For example, from a horizontal jitter perspective, the following example shows two signals that appear to have the same jitter margin (eye opening) when looked at with an oscilloscope, but have significantly different eye openings when studied more deeply. The same is true in the vertical eye opening domain, where the deterministic effects of a lossy channel produce a closed eye much the same way random noise would; however, the Q-factor value between the two cases is substantially different.

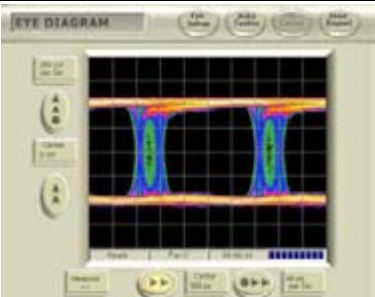
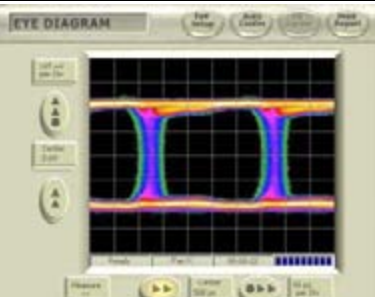
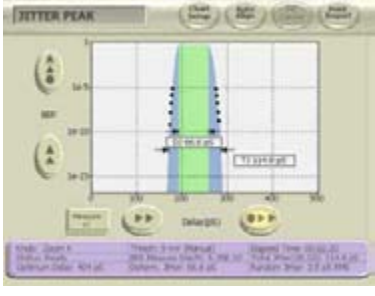


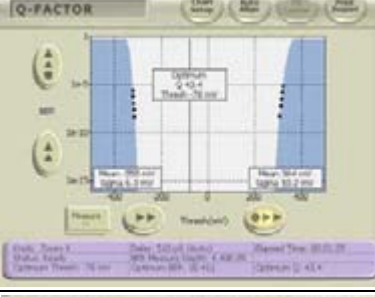
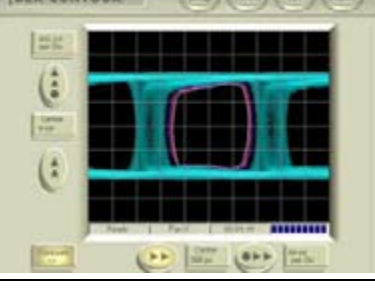
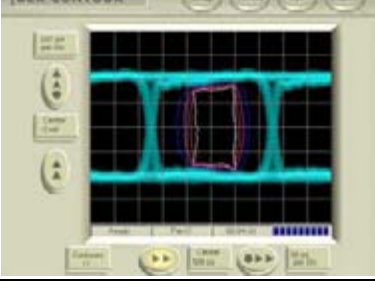
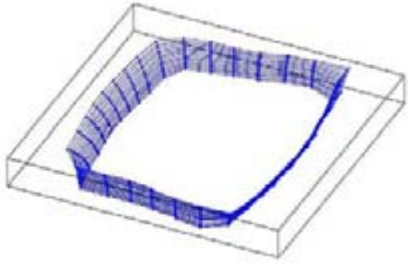
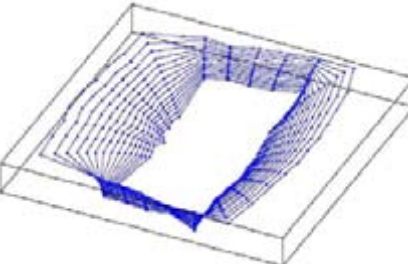
	Deterministic Impairment (Lossy Channel)	Random (Noise-limited)
Eye Diagram		
Jitter Measurement		
Q Factor Measurement		
BER Contour		
BER Contour Plotted in 3-D		

Figure 8: Two different systems with similar looking eye diagrams. Closer inspection shows that the system performance for each will be very different.

Diagnostic Information

When inevitable problems do occur, it is important to have good diagnostic information available to help trace causes. Problems in communications come in many varieties and, depending on their resulting error rate, can be easy or hard to find. When diagnosing problems, it is the job of the engineer to choose which type of tool should be used to attack which type of problem. Often, this is done based on the rate of error occurrences. Problems that happen very frequently are easily viewed using oscilloscopes. However, problems that happen rarely (e.g., at a rate of one in a million or slower) are difficult to observe using sampling methods, especially when triggers occur infrequently.

At these low error rates, error location analysis is the best way to understand the nature of the errors. Error location analysis on the BERTScope assigns a sequential address to all bit errors, and then studies these error locations to find correlations and dependencies that would otherwise be difficult to uncover. Difficult problems such as interference from a switching power supply can easily be found looking at a histogram of error free intervals ('distance' between errors) in the data stream. Error free intervals that match the power supply switching frequency or octaves of this frequency will be evident. Any error free interval that happens more often than others do indicates a systematic error (rather than a random one), and the interval length offers a clue as to the source of the systematic error.

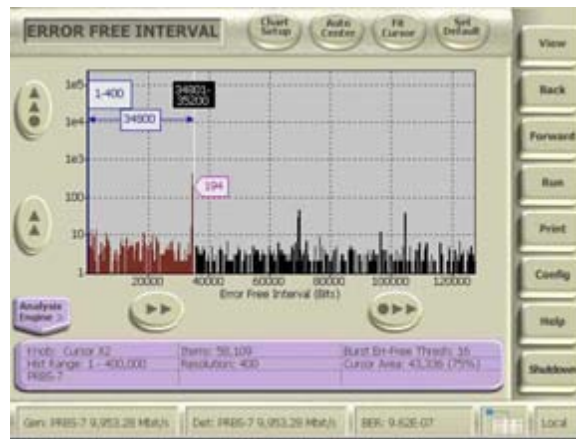


Figure 9: The Error Free Interval histogram clearly shows systematic effects and provides clues such as the frequency of occurrence

For signal integrity issues, remaining bit errors in systems are often the result of either the random components of bit error or the low-level residual from frequency-dependent errors. These tend to cause isolated errors rather than bursts of errors. The BERTScope's ability to separately measure bit error rate from burst error rate when measuring the overall total error rate allows an easy isolation of errors that are probably not due to signal integrity effects — namely, burst errors.



Figure 10: Timeline strip chart of error performance showing bit and burst performance

Burst error definition is adjustable in the BERTScope, as bursts in one application may be different from bursts in another. Experience shows that low-level burst error problems can be some of the most difficult error problems to solve.

When errors are frequency-dependent, then they are also data pattern-dependent. This means that different sections of a test data stream that have varying frequency components will have different probabilities of bit errors. To isolate these types of errors and help debug them, the error location information is correlated to the data pattern information to create a histogram showing the number of bit errors for all locations in the test data pattern.

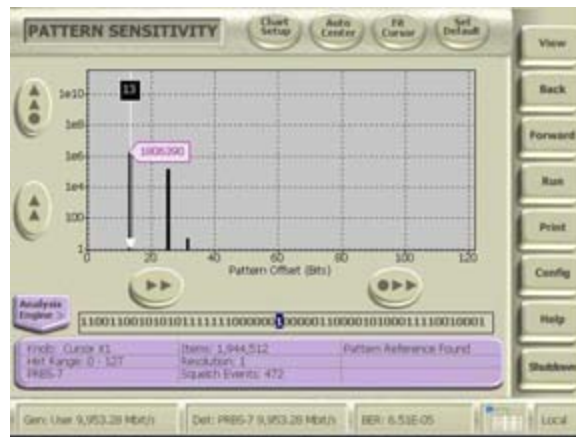


Figure 11: Pattern Sensitivity Analysis showing the most frequent errors in this system occurring on an isolated '1'.

In this example, we see that all detected bit errors fall into only a couple locations in the data pattern, proving the pattern-sensitive nature of this failure. By using the BERTScope's cursor, the expected bit values at these error positions can be shown. Here we see that an isolated single one-bit had the highest probability of an error. This might imply a poor high-frequency response or large baseline wander.

Many different analyses are possible using the bit error location information, including:

Error Free Interval	Identifies systematic errors and gives clues about the frequency component of error.
BER Strip Chart	Separately measures bit and burst error rates and shows trends over time.
Pattern Sensitivity	Shows the probability of having errors at each bit position within the test pattern. Uncovers data-dependent errors.
Correlation	Flexibly correlates error locations to integer or externally triggered boundaries. Uncovers error correlations to parallel busses, multiplexer widths, data frames, etc.
Block Error Analysis	Measures the probability of having various numbers of errors in user-defined block sizes, independent of how close errors are to each other. Ideal for understanding potential retransmit conditions on block error detected data.
Error Mapping	Displays a two-dimensional error map that rasterizes serial error locations based on a raster length set by the user. Appropriate raster lengths are typically uncovered with other analysis techniques, such as Error Free Interval analysis.
Error Correction Emulation	Allows emulation of proposed error correction strategies on actual measured error positions. Block FEC codes, such as Reed-Solomon, are emulated as well as flexible interleaving.

Table 1: Error Analysis types described.

Conclusion

This paper has looked at Signal Integrity measurements with particular attention to the new BERTScope product. Measurements of intrinsic jitter, long-term bit error rate, jitter tolerance, and channel measurements, as well as diagnostic information afforded by the error location analysis features, have been shown. Equipment features such as calibrated stress generators required for compliance testing have been described.

Further, we have seen that Signal Integrity measurements are best done using deep measuring devices such as a bit error rate tester, and that this offers a significant advantage over sampling devices such as oscilloscopes and time interval analyzers.

BERTScopes offer these features in a fully integrated one-unit instrument, with a user interface that is easy for any engineer to use, for data rates up to 7.5 Gbit/sec and 12.5 Gbit/sec.



References

¹ MJSQ - Methodologies for Jitter and Signal Quality Specification, part of the INCITS project T11.2.

<http://www.t11.org/index.htm>

² Example jitter template from XFP industry group: www.xfpmsa.org

³ More information on StatEye can be found at: www.stateye.org