

BERTScope™ PLA

A Complete PLL Compliance
Test Solution For PCIe
Components and Add-In Cards

PCIe PLL Tester

Tools Help

PCIe 2.0

0.5 PHASE MOD (%UI)

AUTOSCALE

OVERLAP TRACES

PCI EXPRESS

- Simple
- Repeatable
- Single Instrument Solution



The Vision of a Scope, the Confidence of a BERT
And Clock Recovery you can Count on.

SYNTHESYS
RESEARCH, INC.



Complete PLL response compliance testing and characterization is quick and easy with the BERTScope PLA – a single instrument solution.

Ease of Use

Of all the methods for testing PLL compliance in PCIe Add-in cards, the BERTScope PLA analysis instruments are the easiest to set up and use. Connect four cables to the Compliance Base Board, plug the instrument's USB cable to any PC, load the software and you are up and testing. No specialized instrument set-ups or calibration runs are required. Pass-Fail determination is just as easy. The simplified user interface allows any user to quickly get the compliance test results they need, without complicated cursor set ups or interpretation that is required using other methods.

The output is presented as a magnitude plot, auto scaled to show the PLL loop response. A parameter bar on the plot shows the direct measurements of the required measurements: PLL -3dB bandwidth and peaking level, along with other useful information.

The BERTScope PLA reference generator always maintains a duty cycle of exactly 50%,

regardless of the amount of frequency modulation. This allows the instrument to test any PLL topology. Other instruments amplitude modulate the 100 MHz reference oscillator, essentially modulating the duty cycle rather than the period. While this technique is adequate for single edge phase detectors, it won't work on the dual edge detectors commonly used to lower clock jitter.

Fast

The instrument sweeps the full range of test frequency in under 15 seconds. Unlike spectrum analyzers, which must reduce the sweep time to achieve good frequency resolution, the BERTScope PLA analysis instrument always maintains full resolution, without slowing down test time. The fast measurement time improves design confidence, by allowing the characterization of a large number of devices, without impacting the design introduction schedule with extra days of characterization time.

Accurate

The BERTScope PLA does not sacrifice accuracy and resolution to achieve ease of use and fast test times. An amplitude measurement resolution of 0.01 dB provides high confidence when testing the peaking limit to the +1 dB allowed by the standard. Other approaches have limited resolution of 0.5 or even 1 dB, limiting the ability to accurately measure peaking and -3 dB bandwidth.

Repeatable

The high measurement resolution and clean reference oscillator provide the granularity required for consistent results – validated through dozens of tests at compliance workshops. Alternative methods with limited resolution can give less repeatable results. Tests made today with the BERTScope PLA will agree with those made last week, or in another lab using a different BERTScope PLA.

Extra tools

While there are other choices of instrument to perform PCIe PLL compliance testing, few provide more than just the compliance test. The BERTScope PLA instruments provide additional measurements useful for the PLL designer to characterize their design. In addition to directly measuring the edge density of the Tx data, the BERTScope PLA provides the option of a phase plot, to see the phase margin of the PLL.

The instrument provides both high resolution and high dynamic range – typically 75 dB. This allows the user to see the transfer of low frequency jitter sources, orders of magnitude below the -3 dB point. The SSC modulation jitter component can be directly measured.

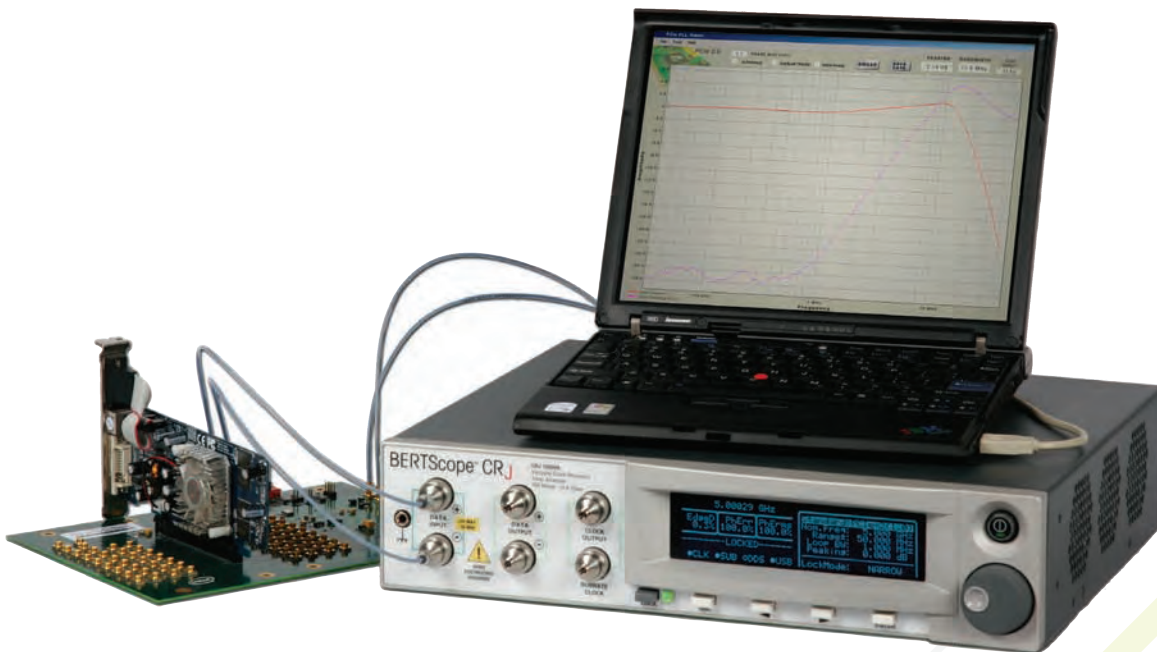
Two Instrument Models to Choose From

The PCIe PLL testing capability is available in the following instrument solutions:

- The CRJ12500A-PCIE (shown below) combines the powerful spectral jitter analysis and instrumentation quality clock recovery functionality of the CRJ12500A with PCIe-PLL analysis. All of the CRJ12500A features and specifications are maintained in the CRJ12500A-PCIE model.
- The PLL-PCIE (shown on page 2) is a cost effective dedicated instrument for PCIe-PLL compliance testing.



A single view provides both the compliance test parameters, along with the PLL loop response and jitter transfer function. No need to change between views to see all of the PLL performance.



Specifications

The following table applies to both the BERTScope PLA CRJ 12500A-PCIE and the PLL-PCIE instruments:

Parameter	Value
Ref. Clock Output:	
General configuration	True differential, compatible with PCI-E electrical specifications.
Base Frequency	100 MHz
Duty Cycle	50% +/- 0.1%
Phase Modulation Frequency	30 kHz to 80 MHz
Modulation amplitude at 100 MHz	0.15 %–1.5 % UI
Residual Phase Jitter	<<43.4 ps integrated from 5 to 16 MHz
Measurement Input:	
General	Differential signal, complies with PCI-Express electrical characteristics
Operating Frequency	2.5 and 5.0 Gbps
Transition Density	62.5% to 75%
Amplitude Resolution	0.01 dB
Frequency Resolution	10 kHz
Relative Amplitude Accuracy	0.05 dB
Measurement Results:	
Plot	PLL loop response magnitude with Jitter Transfer Function and PLL loop response phase.
Parameters	PLL loop—3 dB bandwidth, loop peaking, transition edge density, and data rate.
Hard copy	Results can be printed out in a test report page.
General:	
Dimensions (with connectors and feet, without rack mounting hardware)	Width: 394 mm (15.5") Height: 94 mm (3.7") Depth: 355 mm (14.0")
Weight	Net: 19 kg (14 lbs 10 oz.) Shipping: 12.3 kg (27 lbs)
Temperature	Operating: 0 to +40° C Non-operating: -18 to +60° C
Relative Humidity	Operating: 20 to 80% at or below 40° C Non-operating: 5 to 90% at or below 60° C
Power Requirements	Voltage: 100–240 Vrms Frequency: 50–60 Hz Power: 150 W / 150 VA Max.

The following lists selected additional specifications for the CRJ 12500A-PCIE instrument. Refer to the CR12500A Product Brief for complete specifications.

Parameter	Value
Jitter Spectrum Measurement:	
Jitter Component Frequency Range	200 Hz – 90 MHz
Minimum Frequency Resolution	200 Hz
Maximum Jitter	Limited only by the ability of the clock recovery instrument to lock with PLL BW set at 0.5 MHz and 0.5 dB peaking
Vertical units	% UI or ps
Vertical scale	Linear or Log
Duty Cycle Dependent Jitter:	
Units	% UI or ps
Maximum Range:	50% UI

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PC Requirements:

The BERTScope PLA control and display software operates stand alone on a PC which meets the following minimum requirements:

- USB 2.0 interface
- Display resolution: XGA (1024 x 768) or greater
- Operating System: Microsoft Windows 2000, XP.

Warranty:

BERTScope PLA Instruments are warranted for 1 year.

Ordering Information:

Product Code	Description
PLL-PCIE	BERTScope PLA clock PLL response analyzer for PCIE
CRJ 12500A-PCIE	BERTScope CRJ Clock Recovery Instrument with Jitter and PLL analysis
Extended warranty and product upgrade options are available.	Contact your sales representative for more information.

Included with the PLL-PCIE:

- CD-ROM with BERTScope PLA Control and Display software
 - Interconnecting cables
 - Power cable
 - Instructions for connecting to Compliance Base Board
 - Certificate of Calibration
- Compliance testing the PCIE 5 Gbps specification also requires the Compliance Base Board, ver 2.0. Obtain from the PCIE SIG.

Included with the CRJ 12500A-PCIE:

- CD-ROM with BERTScope PLA Control and Display software
 - Interconnecting cables
 - Power cable
 - 50 Ω Terminators for Data Output connectors when not used (2 each)
 - Instructions for connecting to Compliance Base Board
 - Certificate of Calibration
- Compliance testing the PCIE 5 Gbps specification also requires the Compliance Base Board, ver 2.0. Obtain from the PCIE SIG.

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